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M.Tech. Degree Examination, Dec 08 / Jan 09 Digital Circuits and Logic Design

Time: 3 hrs.

Max. Marks:100

Note : Answer any FIVE full questions.

1.
 - a. Give physical constructional details of threshold element by means of a magnetic core. (06 Marks)
 - b. Discuss the capabilities and limitations of threshold logic. (06 Marks)
 - c. Determine whether the functions :
 $F(x_1, x_2, x_3, x_4) = \sum (0, 1, 3, 4, 5, 6, 7, 12, 13)$ is a threshold functions and if it is, find a weight - threshold vector. (08 Marks)
2.
 - a. Analyze the circuit shown in fig.Q2(a) for static hazards, redesign the circuit so that it becomes hazard free. (07 Marks)

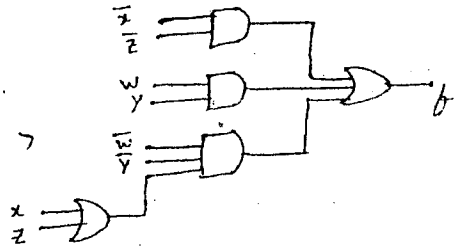


Fig.Q2(a)

- b. Given the fault table shown in table Q2(b), where Z denotes the fault free output for the corresponding test. Find a minimal adaptive fault - location experiment. (07 Marks)

Tests	Faults					Z
	f ₁	f ₂	f ₃ , f ₄	f ₅		
T ₁			1	1	1	0
T ₂	1	1				1
T ₃				1	1	1
T ₄		1				0
T ₅					1	1

Table Q2(b)

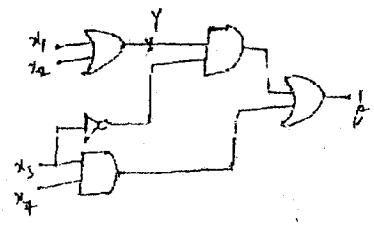


Fig.Q2(c)

- c. For the circuit shown in fig.Q2(c), find tests to detect the fault y s - a - 0 and y s - a - 1. (06 Marks)
3.
 - a. Explain the basic principles of the path sensitization method. (05 Marks)
 - b. Use the map method to find a minimal set of tests for multiple faults for the 2 - level OR - AND network shown in fig.Q3(b). (07 Marks)

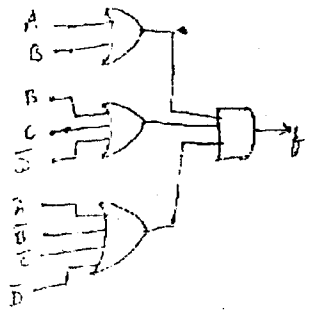


Fig.Q3(b)

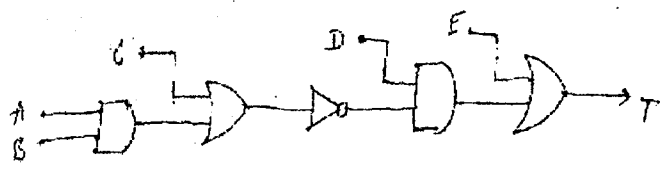


Fig.Q3(c)

- c. Show a quadded logic realization of the circuit shown in fig.Q3(c). Indicate the correction of the longest propagated error. (08 Marks)

- 4 a. Discuss the properties of mealy m/c and moore m/c. (03 Marks)
 b. Find the equivalence partition for the machine shown in table Q4(b). Show a standard form of the corresponding reduced machine. (10 Marks)

P.S	NS, Z	
	x=0	x=1
A	E, 0	D, 1
B	F, 0	D, 0
C	E, 0	B, 1
D	F, 0	B, 0
E	C, 0	F, 1
F	B, 0	C, 0

P.S	NS, Z	
	x=0	x=1
A	A, 0	C, 0
B	B, 0	B, -
C	B, 0	A, 1

Table Q4(c)

Table Q4(b)

- c. Augment the machine shown in Table Q4(c) by state splitting, determine its minimal form. (07 Marks)
- 5 a. For the incompletely specified m/c shown in Table Q5(a), construct the merger table and find the set of all maximal compatibilities. (10 Marks)

P.S	NS, Z	
	I ₁	I ₂
A	E, 0	B, 0
B	F, 0	A, 0
C	E, -	C, 0
D	F, 1	D, 0
E	C, 1	C, 0
F	D, -	B, 0

Table Q5(a)

- b. Given the m/c shown in table Q5(b) and 2 assignments α and β . Derive in each case the logical equations of state variables and output function. Explain how the choice of an assignment affects the complexity of the circuit and determines the overall structure of the m/c. (10 Marks)

P.S	NS		Z	
	x=0	x=1	x=0	x=1
A	A	D	0	1
B	A	C	0	0
C	C	B	0	0
D	C	A	0	1

Assignment α : Assignment β :
 $A \rightarrow 00$ $A \rightarrow 00$
 $B \rightarrow 01$ $B \rightarrow 01$
 $C \rightarrow 11$ $C \rightarrow 10$
 $D \rightarrow 10$ $D \rightarrow 11$

- 6 a. Define the following : i) Closed partition ii) Input consistent partition iii) Output consistent partition iv) Autonomous clock and determine the same for the m/c shown in table Q6(a). (12 Marks)

P.S	NS, Z	
	x=0	x=1
A	E, 0	E, 0
B	D, 0	F, 1
C	F, 0	D, 1
D	A, 0	C, 0
E	C, 0	A, 0
F	B, 0	B, 1

Table Q6(a)

P.S	NS, Z	
	x=0	x=1
A	B, 0	C, 0
B	A, 1	F, 1
C	F, 1	E, 0
D	F, 1	E, 1
E	G, 0	D, 0
F	D, 0	B, 0
G	E, 1	F, 0

Table Q6(b)

- b. Define closed implication graph and construct the same for the m/c shown in table Q6(b) by identifying the pair of states (A,B). (08 Marks)

- 7 a. Find the set of Mm pairs for the m/c shown in table Q7(a)

(10 Marks)

P.S	NS				Z
	x_1, x_2				
	00	01	11	10	
A	C	A	D	B	0
B	E	C	B	D	0
C	C	D	C	E	0
D	E	A	D	B	0
E	E	D	C	E	1

Table Q7(a)

P.S	NS, Z	
	$x = 0$	$x = 1$
A	B, 0	A, 0
B	B, 1	C, 1
C	A, 1	D, 0
D	C, 0	A, 1

Table Q7(b)

- b. Define homing sequence. Find the shortest homing sequence for the m/c shown in table Q7(b). (10 Marks)

- 8 a. The m/c shown in table Q8(a) is initially provided with an input sequence 0 1 to which it responds by producing an output sequence 1 0. It is next provided with the sequence 1 0 1 0 1 0 1 0 1 0 0 1 0 0 1 1 0 1 0 0 0 1. Show that this sequence is a fault – detection experiment for this m/c and find the correct output sequence. (10 Marks)

P.S	NS, Z	
	$x = 0$	$x = 1$
A	A, 1	B, 0
B	C, 0	A, 0
C	B, 0	C, 1

Table Q8(a)

P.S	NS, Z	
	$x = 0$	$x = 1$
A	A, 0	B, 0
B	A, 0	C, 0
C	A, 0	D, 0
D	A, 1	A, 0

Table Q8(b)

- b. Show the testing graph for the m/c given in table Q8(b). Add to the m/c one output terminal so that the sequence 1 1 will be a distinguishing sequence. (10 Marks)

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M.Tech. Degree Examination, Dec.09/Jan.10
Digital Circuits & Logic Design

Max. Marks:100

Time: 3 hrs.

Note: Answer any FIVE full questions.

- 1 a. Explain the concept of threshold logic. (05 Marks)
- b. Determine the function $f(x_1, x_2, x_3, x_4)$ realized by the network shown in Fig.1(b). (06 Marks)

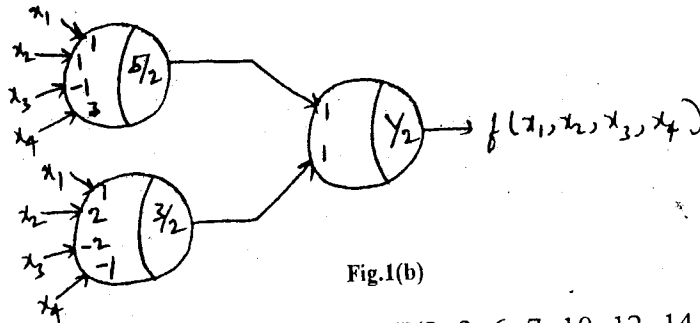


Fig.1(b)

- c. Given the switching function $f(x_1, x_2, x_3, x_4) = \Sigma(2, 3, 6, 7, 10, 12, 14, 15)$. Find a minimal threshold logic realization. (09 Marks)

- 2 a. For the circuit shown in Fig.2(a), wires m, n, p & q may become either s-a-0 or s-a-1. Determine a minimal fault-detection experiment by means of fault table. (10 Marks)

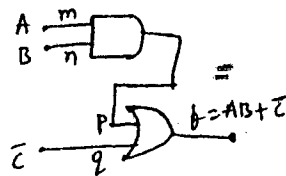


Fig.2(a)

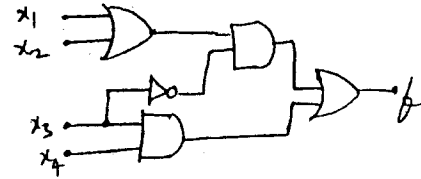


Fig.3(a)

- b. What are critical and sub-critical errors? Determine the same for AND, OR, NAND, NOR & EX-OR gates. (05 Marks)
 - c. With a net diagram, explain the basic structure of a quadded network. (05 Marks)
- 3 a. For the circuit shown in Fig.3(a), find all tests to detect the faults x_3 , s-a-0 & x_3 s-a-1. (10 Marks)
 - b. Use the map method to find a minimal set of tests for multiple faults for the two-level AND-OR realization of the function $f(w, x, y, z) = w\bar{z} + x\bar{y} + \bar{w}x + w\bar{x}y$ (10 Marks)
- 4 a. For the m/c shown in Table 4(a), find the equivalence partition and a corresponding reduced m/c in standard form. (10 Marks)

Table 4(a)

P.S.	NS, Z	
	x = 0	x = 1
A	F, 0	B, 1
B	G, 0	A, 1
C	B, 0	C, 1
D	C, 0	B, 1
E	D, 0	A, 1
F	E, 1	F, 1
G	E, 1	G, 1

remaining blank pages. :g. 42+8=50, will be treated as malpractice
 Important Note: 1. In completing your answers, compulsorily draw diagonal cross lines
 2. Any revelation, appeal to evaluator and/or equations

- b. Draw the merger graph and compatibility graph and determine the minimal closed covering for the m/c shown in Table 4(b). (10 Marks)

Table 4(b)

P.S.	NS, Z			
	I ₁	I ₂	I ₃	I ₄
A	-	-	E, 1	-
B	C, 0	A, 1	B, 0	-
C	C, 0	D, 1	-	A, 0
D	-	E, 1	B, -	-
E	B, 0	-	C, -	B, 0

- 5 a. The m/c shown in Table 5(a) has the following closed partitions. $\pi_1 = \{\overline{ACE}; \overline{BDF}\}$, $\pi_2 = \{\overline{AF}; \overline{BE}; \overline{CD}\}$.

- i) Find a state assignment which reduces the interdependencies of the state variables.
 ii) Derive the logical equations and show the circuit diagram when unit delays are used as memory elements. (10 Marks)

Table 5(a)

P.S.	NS		Z
	x = 0	x = 1	
A	D	C	1
B	A	D	0
C	B	E	0
D	E	B	0
E	F	C	0
F	C	D	0

- b. For the m/c shown in Table 5(b) find the π - lattice. (10 Marks)

Table 5(b)

P.S.	NS	
	x = 0	x = 1
A	D, 0	C, 0
B	C, 0	D, 1
C	E, 0	F, 0
D	F, 0	F, 1
E	G, 0	H, 0
F	H, 0	G, 1
G	B, 0	A, 0
H	A, 0	B, 1

- 6 a.

Table 6(a)

P.S.	NS		Z	
	x = 0	x = 1	x = 0	x = 1
A	D	B	0	0
B	A	C	1	0
C	B	E	1	0
D	F	A	0	1
E	F	C	0	0
F	E	D	0	1

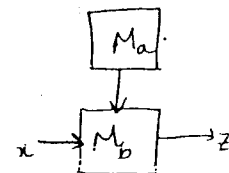


Fig.6(a)

- i) Determine state assignment for the m/c shown in Table 6(a) so that it will have the structure shown in Fig.6(a).
 ii) Show the state diagram of the input-independent component. (10 Marks)

b.

P.S	NS			Z
	x ₁ x ₂	01	10	
A	C	B	D	0
B	A	E	C	0
C	E	B	D	0
D	C	C	E	0
E	E	D	B	1

Table 6(b)

Determine the set of all Mm pairs for the machine shown in Table 6(b)

(10 Marks)

- 7 a. For the m/c shown in Table 7(a), determine the synchronizing tree and synchronizing sequence to synchronize the m/c to state D. (10 Marks)

Table 7(a)

P.S.	NS, Z	
	x = 0	x = 1
A	B, 0	D, 0
B	A, 0	B, 0
C	D, 1	A, 0
D	D, 1	C, 0

- b. For the m/c shown in Table 7(b) construct the distinguishing tree. Obtain all possible distinguishing sequences. Write the response of m/c to the sequence 111. (10 Marks)

Table 7(b)

P.S.	NS, Z	
	x = 0	x = 1
A	C, 0	D, 1
B	C, 0	A, 1
C	A, 1	B, 0
D	B, 0	C, 1

- 8 a. Identify the m/c which is known to have two states and its response to the i/p sequence X is the o/p sequence Z, as shown below:

Time :	t ₁	t ₂	t ₃	t ₄	t ₅	t ₆	t ₇	t ₈
X:	1	1	1	0	1	0	1	
Z:	0	1	0	0	1	0	0	

(10 Marks)

- b. What is a diagnosable sequential m/c? Construct testing table and graph for the m/c shown in Table 8(b). (10 Marks)

Table 8(b)

P.S.	NS, Z	
	x = 0	x = 1
A	B, 0	D, 0
B	A, 0	B, 0
C	D, 1	A, 0
D	D, 1	C, 0

M.Tech. Degree Examination, May/June 2010

Digital Circuits and Logic Design

Time: 3 hrs.

Max. Marks:100

Note: Answer any FIVE full questions.

- 1 a. Find the function $f(x_1, x_2, x_3, x_4)$ realized by the threshold element shown in Fig.Q1(a). Show the map of the function. (06 Marks)

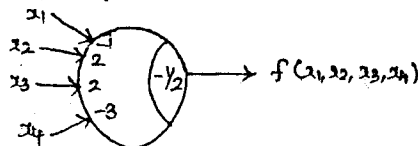


Fig.Q1(a)

- b. Discuss the following : (06 Marks)
 i) Elementary properties ii) Unate function
 c. Determine whether the function $f(x_1, x_2, x_3, x_4) = \Sigma (0, 1, 3, 4, 5, 6, 7, 12, 13)$ is a threshold element, and if it is find the weight threshold vector. (08 Marks)

- 2 a. Explain the static hazard and hazard free circuits, with example. (08 Marks)
 b. Explain the quadded logic, with an example. (06 Marks)
 c. Apply Boolean difference method to test wire 'h' in the circuit shown in the Fig.Q2(c). (06 Marks)

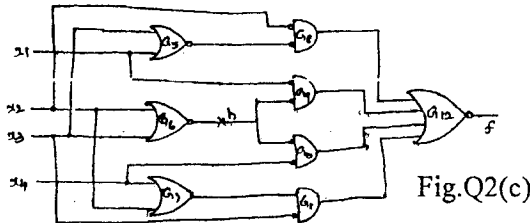


Fig.Q2(c)

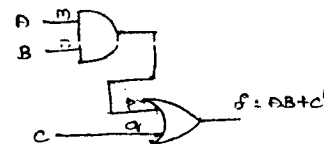


Fig.Q3(a)

- 3 a. Explain and construct the fault table for the circuit shown in Fig.Q3(a). (06 Marks)
 b. Write a note on fault detection by path sensitizing. (06 Marks)
 c. Briefly discuss the following : (08 Marks)
 i) Possible strategies in failure tolerant design ii) Restoring organs.

- 4 a. List the capacities and limitations of finite state machines. (06 Marks)
 b. Discuss the property of Mealy m/c and Moore m/c. (04 Marks)
 c. Find the minimal form of machine M shown in Table.Q4(c) below. Also find its isomorphic machine and deduce its standard form. (10 Marks)

PS	NS, z	
	x = 0	x = 1
A	E, 0	C, 0
B	C, 0	A, 0
C	B, 0	G, 0
D	G, 0	A, 0
E	F, 1	B, 0
F	E, 0	D, 0
G	D, 0	G, 0

Table.Q4(c)

- 5 a. What is merger graph? Draw the merger graph for the incompletely specified machine M1 shown in Table.Q5(a). (10 Marks)

PS	NS, z			
	I ₁	I ₂	I ₃	I ₄
A	-	C, 1	E, 1	B, 1
B	E, 0	-	-	-
C	F, 0	F, 1	-	-
D	-	-	B, 1	-
E	-	F, 0	A, 0	D, 1
F	C, 0	-	B, 0	C, 1

Table.Q5(a)

PS	NS, z	
	x = 0	x = 1
A	A, 0	C, 0
B	B, 0	B, -
C	B, 0	A, 1

Table.Q5(b)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
 2. Any revealing of identification, appeal to evaluator and/or equations written eg, 42+8 = 50, will be treated as malpractice.

5 b. What are compatible states? For the tabular column Table.Q5(b) shown machine 'M', find the augmented machine and corresponding minimal machines. (10 Marks)

6 a. Given the machine M shown in Table.Q6(a) and the two assignments α and β , derive in each case the logical equations for the state variables and the output function and compare the results. Draw the circuit and block diagram corresponding to both the assignments.

PS	NS,		z	
	x=0	x=1	x=0	x=1
A	A	D	0	1
B	A	C	0	0
C	C	B	0	0
D	C	A	0	1

$$\alpha = \begin{bmatrix} 0 & 0 \\ 0 & 1 \\ 1 & 0 \end{bmatrix} \quad \beta = \begin{bmatrix} 0 & 0 \\ 0 & 1 \\ 1 & 0 \\ 1 & 1 \end{bmatrix}$$

Table.Q6(a)

(10 Marks)

b. Explain input independence and autonomous clock. For the machine 'M' shown in Table.Q6(b), find input consistent partition. If the assignments are as follows, find the logical equation for machine.

PS	NS,		z	
	x=0	x=1	x=0	x=1
A	D	C	0	1
B	C	D	0	0
C	E	F	0	1
D	F	F	0	0
E	B	A	0	1
F	A	B	0	0

Table.Q6(b)

Assignments

- A → 000
- B → 001
- C → 010
- D → 011
- E → 100
- F → 101

Draw the realization of machine 'M' using autonomous clock and draw the autonomous clock of machine M. (10 Marks)

7 a. What are covers and implication graph? For the machine 'M' shown in Table.Q7(a), the closed partition by state splitting. Write the corresponding logical equations and also the implication graph.

PS	NS		Z	
	x=0	x=1	x=0	x=1
A	A	B	0	1
B	C	B	0	0
C	A	C	0	0

Table.Q7(a)

(10 Marks)

b. What is a tree? Explain the types of tree. (05 Marks)

c. Draw the homing tree of the machine 'M' shown in the Table.Q7(c) and explain it. Write the response of machine 'M' to the homing sequence 010. (05 Marks)

PS	NS, z	
	x=0	x=1
A	B, 0	D, 0
B	A, 0	B, 0
C	D, 1	A, 0
D	D, 1	C, 0

Table.Q7(c)

8 a. What is an experiment? Explain the types of experiment. (05 Marks)

b. Prove the theorem:

If an n-state machine has a synchronizing sequence, or sequences, then it has one such sequence

whose length is at most $\frac{n(n+1)(n-1)}{6}$. (10 Marks)

c. Write a short note on machine identification. (05 Marks)
